

Designing a cellular low power DDR non-volatile memory system

with Numonyx™ Velocity LP™ NV-RAM

LPDDR-NVM interface standard delivers cellular enhancements

Read performance improvements

Pin count reduction

Control interface space management

Scalability

Designing a cellular low power DDR non-volatile memory system

Cellular phone systems continue to rely on NOR flash memory to deliver high read bandwidth to run application code. For current eExecute-In-Place (XIP) systems, NOR flash devices are used to run application code, and high-speed SDRAM is used for frequently accessed data. To increase memory throughput performance, many cellular memory systems now use LPDDR SDRAM as the main system memory for data. This practice creates a memory infrastructure that requires at least two separate buses, one for SDRAM and one for flash.

Cellular systems benefit from features of LPDDR interface

Numonyx™ Velocity LP™ NV-RAM, the first NOR flash device to reside on an LPDDR bus, is an innovative solution for future cellular memory systems. By combining the execution memories in the system onto one interface, Numonyx Velocity LP enables a reduction in pin count, as well as a reduction in overall system complexity (single memory interface, less traces on the board). When packaged with other memories, Numonyx Velocity LP has the ability to scale from low-end to high-end cellular memory systems while keeping the cost at a minimum, as a result of the elimination of a dedicated bus for NOR flash.

Read performance improvements

Numonyx Velocity LP is capable of achieving higher read bandwidths than traditional NOR flash devices due to its ability to interleave read commands. In traditional NOR flash devices, read commands must be

completely serialized. (Figure 1) Subsequent read commands cannot begin until uncompleted read commands have been completed. Interleaving read commands using Numonyx Velocity LP architecture allows for shadowing of some initial access delays, resulting in a reduced overall initial access delay. This is achieved by using Numonyx Velocity LP Row Data Buffers (RDBs). Numonyx Velocity LP utilizes four RDBs, which act as an internal cache to store Row Data after it has been sensed from the array. Once a row has been activated from the array, it remains in the RDB, where it will have a CAS Latency (CL) of three clocks. While an RDB entry is being read, an ACTIVATE command may be issued to activate an additional Row into an alternate RDB entry. Hence, some of the RAS delay may be reduced by overlapping RAS and CAS delays. Furthermore, the improvement seen is much greater when subsequent READ commands address rows that have been previously placed in the RDB. This would equate to a page hit.

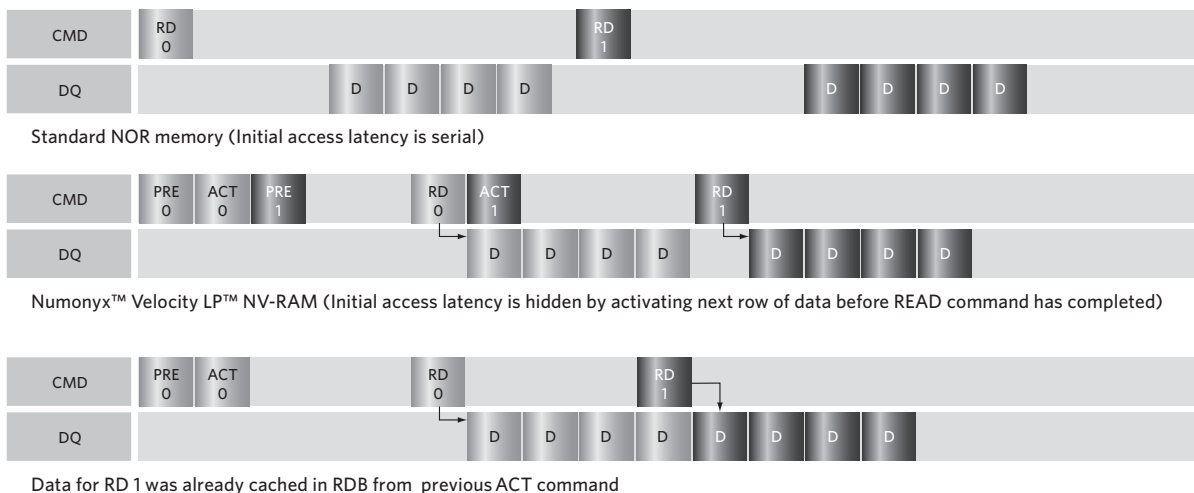


Figure 1: Read data returns comparison for standard NOR flash versus Numonyx™ Velocity LP™ NV-RAM

Pin count reduction

An additional benefit of using Numonyx Velocity LP, rather than a traditional NOR flash, is that a dedicated NOR flash bus can be eliminated. Figure 2 illustrates a generic cellular phone memory system which uses a Numonyx™ StrataFlash® Cellular Memory (M) NOR device for application code storage.

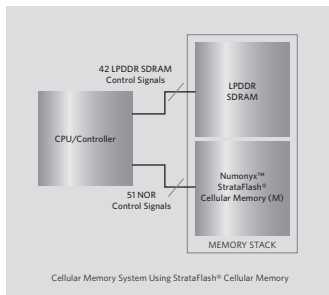


Figure 2: Cellular memory system NOR flash configuration

With the inclusion of LPDDR SDRAM in memory systems, a dedicated bus is required for standard NOR flash devices which cannot share the LPDDR bus. This comes at a cost of 51 control pins for a StrataFlash memory device. With its split bus system, Numonyx Velocity LP only requires 42 pins for control, reducing the number of control pins by 9. (Figure 3) The elimination of a dedicated NOR flash bus reduces the overall system cost due to the lower pin count and reduces the overall system board layout complexity as less traces are required on the board.

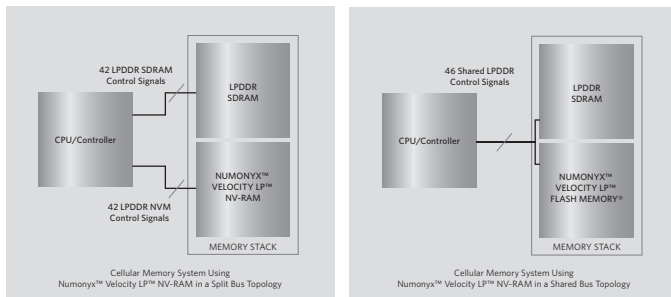


Figure 3: Cellular memory systems NOR flash configurations

Control interface space management

Numonyx Velocity LP utilizes a dynamically allocated control space. The Overlay Window (OW) is a movable set of control registers which may be dynamically placed anywhere within the flash array space. (Figure 4) The flexibility of the OW allows system designers to place boot code anywhere within the flash array without concern about the logical location of the flash control interface. The Overlay Window Base

Address is set through a Mode Register Set (MRS) command which may be enabled and disabled to eliminate the loss of any address space in the array.

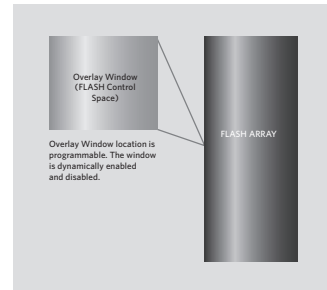


Figure 4: Flash control space management

Scalability

Numonyx Velocity LP can be stacked with LPDDR SDRAM in a package and share a 32-data lane or a 16-data lane bus, offering full scalability for high-end to low-end cellular systems.

As an example, a premium high-end system may require two or more dedicated 32-data lane memory buses for bandwidth intensive applications. In this scenario, one memory interface is dedicated for core applications such as running the OS, while other dedicated memory interfaces would be used for peripherals such as graphics and I/O. With Numonyx Velocity LP, the NOR flash would share the main system memory bus with a 32-data lane LPDDR SDRAM memory device for an XIP stack. (Figure 5) The peripheral memory bus would consist of a dedicated 32-data lane LPDDR SDRAM for running graphics applications. An additional NAND bus may be required for data storage as well as additional room for data storage memory upgrades.

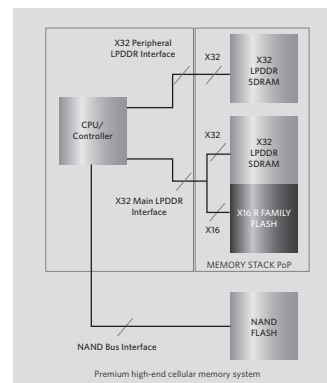


Figure 5: Premium high-end cellular memory system with two dedicated X32 LPDDR memory buses

Low power DDR cellular memory system

A typical high-end system may require two dedicated 16-data lane memory buses. (Figure 6) Similarly, one bus would be dedicated for core applications while the secondary bus would be dedicated to peripheral applications. Because Numonyx Velocity LP is a 16-data lane device, sharing the bus with a 16-data lane LPDDR SDRAM would reduce the overhead of the extra data lanes of a 32-data lane bus when accessing data from flash. Additionally, NAND flash memory buses would be added to support data storage and data storage upgradeability.

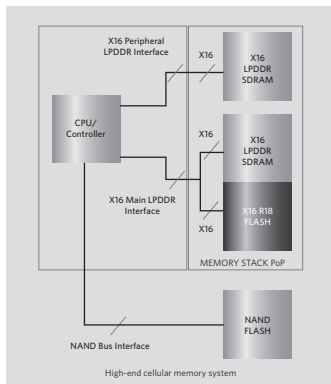


Figure 6: High-end cellular memory system with two dedicated X16 LPDDR memory buses

In mainstream cellular systems, only one memory interface may be used. Numonyx Velocity LP would be used for code storage in an XIP stack. An LPDDR NOR/LPDDR SDRAM/NAND combination can be stacked together into one package to create a complete memory platform. In this scenario, the LPDDR interface may consist of 16 or 32 data lanes. (Figure 7)

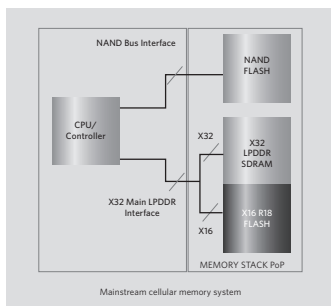


Figure 7: Mainstream cellular memory solution with one dedicated LPDDR memory bus

Finally, Numonyx Velocity LP can be integrated in low-end cellular systems where an LPDDR NOR/LPDDR SDRAM stack can be packaged together for a complete memory system hierarchy. (Figure 8)

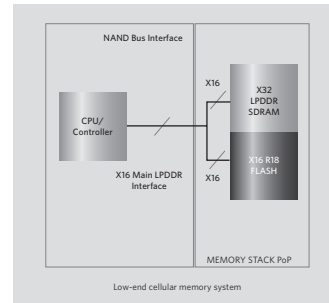


Figure 8: Low-end cellular memory solution with one dedicated LPDDR memory bus

Conclusion

With the demand for bandwidth ever increasing on cellular applications, the migration towards LPDDR devices will continue to progress. The introduction of the Numonyx Velocity LP NV-RAM product family will add a great benefit to platform designs using an LPDDR memory architecture. The addition of an LPDDR-NVM solution will greatly improve memory performance while maintaining lower system costs. Numonyx Velocity LP eliminates the need for a dedicated NOR bus, while also lowering the pin count requirements. Reading out data at double the clock rate will also tremendously improve performance over other NOR flash devices.

For more information regarding Numonyx Velocity LP NV-RAM product family, please contact your Field Sales Representative. Or visit numonyx.com.